REMARKS

The Examiner appears to be asserting that the information disclosure statement (IDS) of 4/26/2002 does not comply with 37 CFR 1.98(a)(1), which requires a list of cited materials. The Applicants respectfully disagree, since the cited pending application was listed at the bottom of page 1 of the IDS. This application has since issued as US Patent 6,567,912. An IDS citing the issued patent has been submitted herewith and a fee paid. However, the Applicants submit that this second IDS submission is superfluous and request that a refund of the IDS fee be credited to Deposit Account No. **502117 -- Motorola, Inc.**

Claims 1, 2, 4, 6-8, 9, 11, 13 and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Buckland et al. (U.S. Patent Number 5,815,647, hereinafter "Buckland"), claims 3 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckland in view of Richardson et al. (U.S. Patent Number 4,131,945, hereinafter "Richardson"), and claims 5 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckland. The applicant respectfully disagrees with these rejections and requests reconsideration.

Claims 1 and 8 recite "a power-up sequence." However, Buckland does not appear to discuss a power-up sequence of peripheral components. The Examiner refers to Buckland Fig. 6, element 108a as teaching a "next peripheral component." The accompanying text, Buckland column 6, lines 11-26, reads (emphasis added):

> Mezzanine bus 102 is connected to at least one PCI to PCI bridge chip 104. This chip provides the interface between the I/O bus and the actual adapter slot 106 which includes a connector 4 and additional logic. Slot 106 will receive an I/O device 108, which may be resident on device 5. The PCI architecture and specifications are available from the PCI Special Interest Group (PCI-SIG), hereby incorporated by reference. The present invention adds additional control logic as shown by reference numeral 105, but does not require modification of the PCI architecture. It should be noted that most computer systems will include **more than one I/O slot, as shown in FIG. 6. The additional slots are represented by adding the letter "a" to the reference numerals which are used to describe the components of the present invention.**

However, Buckland only seems to discuss multiple peripheral components, not a power-up sequence of peripheral components as claimed.

Claims 1 and 8 recite storing an identifier of a first peripheral component and applying power to a next peripheral component when an indication that the first peripheral component has initialized is received. The Examiner cites web pages that discuss PCI and ESCD in addition to Buckland as teaching this claim language. However, the Applicants do not see where these references teach storing or applying power **when an indication that the first peripheral component has initialized is received**. It is when the information is stored in the power-up sequence that is of great importance to the claimed operation as a whole. Thus, the **Applicants request the Examiner to explain specifically how the cited references allegedly teach or suggest when storing and applying power occur**. The Applicants respectfully submit that they do not.

Claims 1 and 8 recite restarting the power-up sequence and skipping the first peripheral in the power-up sequence as a result of determining that an identifier of the first peripheral was not stored when the first peripheral, while initializing, **locks up the bus**. Buckland refers to cards issuing an error signal. However, the Applicants cannot find any reference to locking up a bus, as claimed. In the *Background of the Invention* section of the application, the Applicants discuss bus lock ups as follows:

> Particularly, problematic are failures that lock up a common communication bus that serves many or all of the device cards in a system chassis. These failures effectively disable the entire system and are not remedied by re-initializing the system. Thus, the system is down until the device card can be manually replaced or at least removed, likely impacting user services for a significant period of time.

The Applicants submit that the fact that a card in Buckland can issue an error signal indicates that the card has not locked up the bus.

Claims 1 and 8 recite restarting the power-up sequence and skipping the first peripheral in the power-up sequence as a result of determining that an identifier of the first peripheral was not stored when the first peripheral, while initializing, locks up the bus. The Examiner seems to cite Buckland as teaching this claim language. However,

the Applicants do not see where this reference teaches **skipping the first peripheral in the power-up sequence** or where it teaches restarting and skipping **as a result of determining that an identifier of the first peripheral was not stored**. Thus, the **Applicants request the Examiner to explain specifically how the cited references allegedly teach or suggest this claim language**. The Applicants respectfully submit that they do not. For example, the Examiner cites steps 4-9, 11, and 12 of Fig. 10. The accompanying text, Buckland column 12, line 55 - column 13, line 54, reads (emphasis added):

> FIG. 10 is a flow chart showing the steps implemented by the error recovery aspect of the present invention. At step 1 the process is started and at step 2 the device driver performs any load/store operations to the the device being controlled. It should be noted that the present invention also addresses the situation wherein a string, or related group, of load/store operations are to be implemented. Step 3 then determines whether an SERR# signal is present from one of the plurality of devices on the adapter cards in the computer system. If so, then at **step 4**, the reset signal RST# is activated (by bridge chip 104) to the device signaling SERR#, to place the device 5 in its reset state and avoid any damage to the system, while still keeping the device coupled to the system. That is, the slot 106 having the feature card which issued the SERR# signal is reset in the manner as previously described (data processing activity is ceased). At **step 5**, the status bit in register 203 is set, e.g. to logical 1. Next, at **step 6**, the control hardware as shown in FIG. 9 will ignore all load and store operations, and abort any pending direct memory access (DMA) operations. If at step 3 it was determined that there was no SERR# present, then the process of the present invention continues to **step 7** where it is determined if there are additional load and store operations in the string of instructions being implemented. If there are additional load and/or stores, then the process loops back to step 2 where the device driver implements the load/store. If there are no additional load/store operations, then at **step 8** the device driver reads the status bit in register 203 of bridge chip 104. **Step 9** then determines if an error condition has occurred. If at step 5, the status bit was not set to indicate that an SERR# error has occured, then the load/store operations are considered to have completed (step 10). However, if at step 5 the status bit was set to indicate the presence of an SERR# signal, then bridge chip 104 is reconfigured (by re-initialization) at **step 11**. Typically, the device driver will reset the feature card by re-initializing the device. However, the present invention contemplates that the device driver may also attempt a retry operation that would tell the bus master device which is attempting to transfer information between itself and the device to attempt the transfer operation again. If the error condition has been removed, then the load/store operation may be implemented correctly. Further, at **step 11**, the device driver may call one or more service routines which will attempt to correct the error condition in the device. These error routines may reside in computer's read only memory (ROM) as part of the power on self test (post) code, or the like. However, **the typical situation is for the device driver to re-initialize the device having the error condition**. In accordance with

the present invention, only the particular device which actually generates the error code with be re-IPLed. The remaining devices on the plurality of feature cards in the computer system will continue normal data processing activities. Thus, it can be seen how the present invention allows a computer system to isolate a single device in a particular I/O slot 106, without affecting the operations of other devices on other cards 5 in different slots.

At **step 12, the particular device generating the error code is then re-initialized by the device driver**. The device driver is then set back to a checkpoint state for normal data processing activies (step 13). That is, the device driver has initialized the device and is controlling its activities in a normal manner, e.g. by implementing load and store operations to transfer information between itself and the device being controlled. This also includes determining when an SERR# signal has occurred in the device being controlled, as shown by step 3. It can be seen that subsequent to step 13 the process loops backs to step 2 and continues.

Moreover, as seen in the passage quoted above, Buckland seems to teach away from claims 1 and 8. At step 12, Buckland says that "**the particular device generating the error code is then re-initialized by the device driver**" (emphasis added). In contrast, claims 1 and 8 describe **skipping** the first peripheral in the power-up sequence. Specifically, claim 1 recites "skipping the first peripheral component in the power-up sequence as a result of the step of determining **to prevent the bus from being locked up**." Again, these divergent actions serve to illustrate that Buckland addresses a substantially different problem than the present application does. Thus, the Applicants submit that Buckland cannot be "stretched to fit" what is described in the claims of the present application.

Since neither Buckland nor Richardson, either independently or in combination, teach all of the limitations of base claims 1 and 8, or therefore, all the limitations of their dependent claims, the applicants assert that the Examiner has not shown anticipation nor made a prima facie case for obviousness. No remaining grounds for rejection or objection being given, the applicant now respectfully submits that the claims in their present form are patentable over the prior art of record, and are in condition for allowance. As a result, allowance and issuance of this case is earnestly solicited.

The Examiner is invited to contact the undersigned, if such communication would advance the prosecution of the present application. Lastly, please charge any additional fees (including extension of time fees) or credit overpayment to Deposit Account No. **502117 -- Motorola, Inc**.

Respectfully submitted,
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By: _____

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